RTL2GDSII Flow

Processors are like the brain of a technology that gives directions and instructions to peripheral devices telling them to send information collected from the real world so that it can process that information and in return give processed information back to the external environment.

Usually, the RTL2GDSII flow takes anywhere from 14-16 months and just for fabrication, the foundries take 4-6 months to receive the GDSII file and give a chip in hand.

There are various steps to be followed to create a GDSII file for a specific application, here I have described each process briefly –

1. First, we must find the application that we want the chip to do. It can be anything from TVs, Acs, watches, microcontrollers etc. After finding the application, we must test its working using a GCC compiler. A GCC compiler is a C compiler that is used in Linux. Upon testing, we get a measured output O0.
2. Next, we model the specification of the processor that we are going to build for the application mentioned and test whether the application runs on the specification of the processor. Upon testing we get a measured output O1. Our goal is to achieve O0 = O1.
3. With the above process completed, we now move onto writing the code for our hardware using any HDL like Verilog. Now, we test the application on the hardware code and measure another output O2. We have to make sure that O1 = O2.
4. From here on, our SoC design flow starts and comprises of mainly two modules –
   1. Processor – Code written must be synthesizable (Code can be directly converted into gates)
   2. Peripherals/IPs
      1. Macro – Modules that are repeated multiple times/instantiated in the code multiple times. This need to be synthesizable too.
      2. Analog IPs – They are the functional in nature meaning that don’t have too synthesizable. They are replaced by MOSFETs in the end. A few examples of Analog IPs are 10-bit ADC, PPL, DAC etc.
5. After this you integrate the SoC with GPIO pins (General Purpose Input Output) which acts as the medium of communication for signals to enter and leave the microprocessor. We test our application on the integrated chip and measure an output O3. Our main goal for this step it to get O1 = O2 = O3.
6. Next step is more in backend. Here we perform various steps like Floor planning, Power planning, Placement, CTS and Routing.
7. After this we get out GDSII file (Graphical Data Stream Information Interchange) that will be done through various tests like DRC/LVS and is then sent to the foundries for fabrication. This process of sending the GSDII file to foundries is called TAPEOUT.
8. After fabrication of chips and further tests, it is sent back to the designer and that is called TAPEIN. Once chips are taped in, we must write firmware and software codes to collect information from the external environment and see if the processor is working as we expected it to. We run the application on the completed board containing Processor, Peripherals, GPIOs and measure an output O4.  
   The main goal here is to have out O1 = O2 = O3 = O4. If we are able to achieve this then it can be said that, the chip designed and fabricated works for the specifications mentioned.

This tells us the entire design flow using by current industry and having a more hands on experience with boost your resume and skills that will help you with your career.